PATENT
DOCKET: CU-3300

Remarks/Arguments

Claims 1, 3, 5, and 13-22 are pending in the present application. By the present amendment, claim 1 has been amended. No new matter has been added.

In the office action mailed May 25, 2010, claims 1, 3, 5, and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over US 2003/0117456 (Moon) in view of US 5,764,212 (Nishtani).

The applicant thanks the examiner's response to the applicant's earlier argument that the cited Moon reference cannot and does not teach the claimed --sequence recognition unit--. The applicant does not agree, but, regardless, the applicant respectfully wishes to distinctly point out that Moon and the presently claimed invention are quite different from each other.

The applicant has already pointed out the following in the last filed amendment that the presently claimed invention solves the problems associated with the voltage drops in the signal line pattern 22 as shown in FIG. 2 (Prior Art). For example, referring to FIG. 7, there would be voltage drop of Vs = Ig x Rp across the gate driver IC 44 (where Ig is the current and Rp is the overall resistance). To solve this problem, the presently invention teaches specifically --a gate on-off voltage generation unit-- that can adjust the voltage by, for example, by **subtracting** a **voltage attenuation quantity** corresponding to the location data of the gate driver IC from the first gate-off voltage **without use of a compensating resistor to generate the voltage attenuation quantity**. The applicant emphasizes again that **no** compensation resistor is required or used in a gate driver IC to adjust for the voltage drop across. Rather, the voltage value to be offset (e.g., the voltage attenuation quantity) is generated according to, inter alia, --the location data-- of the gate driver IC.

In the Background section of the specification page 6, line 19 to page 7, line 3, the presently invention specifically rejects using resistors inside signal line patterns in gate driver ICs, because this will create design problems in that the design of the gate driver ICs must be changed every time according to several variables.

The applicant respectfully refers again to Moon [0055], in which Moon specifically teaches using "**a compensating resistor ... within each of the gate driver ICs 48A to 48D.**" Moon clearly teaches using "compensating resistance values for each of the compensating resistors" in [0056 towards the end of the paragraph], and there are no other disclosure in Moon

other than [0055] and [0056] that addresses the problems related to compensating for voltage difference.

To further clearly emphasize this difference, claim 1 has been amended as follows:

> --a gate on-off voltage generation unit for receiving a first gate-off voltage and the location data of the pertinent gate driver IC, and outputting a second gate-off voltage which is generated by subtracting a voltage attenuation quantity corresponding to the location data of the gate driver IC from the first gate-off voltage **without use of a compensating resistor to generate the voltage attenuation quantity**--.

Clearly, for the reasons above, Moon does not teach claim 1 as amended, and allowance of all pending claims 1, 3, 5, and 13-22 are respectfully requested in the next action. The examiner is encouraged to contact the undersigned attorney by telephone to resolve any issues remaining.

Respectfully submitted,

Dated: August 24, 2010

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